SCELBI
QUICK REFERENCE

Version 1.6

TO START UP SCELBI 8H

JUMP to 070 070
(no memory present, reads 377, halt)

TO JAM SINGLE BYTE INSTRUCTION

1: SET INSTRUCTION CODE ON PANEL
2: PUSH INTERRUPT SWITCH
3: STEP UNTIL INTERRUPT LED GOES ON
4: STEP UNTIL INTERRUPT LED GOES OUT

TO JAM TWO BYTE INSTRUCTION

1: SET INSTRUCTION CODE ON PANEL
2: PUSH INTERRUPT SWITCH
3: STEP UNTIL INTERRUPT & LEFT STATUS ON
4: SET DATA CODE ON PANEL SWITCHES
5: STEP AGAIN

TO JAM THREE BYTE INSTRUCTION

1: FOLLOW TWO BYTE PROCEDURE
2: SET SECOND DATA CODE ON PANEL
3: STEP AGAIN

TO LOAD MEMORY

1: LOAD H WITH TARGET ADDRESS (056 XXX)
2: LOAD L WITH TARGET ADDRESS (066 XXX)
3: LOAD MEMORY IMMEDIATE* (076 XXX)
4: INCREMENT L (060)
5: REPEAT STEPS 3 AND 4

TO DUMP MEMORY

1: LOAD H WITH TARGET ADDRESS (056 XXX)
2: LOAD L WITH TARGET ADDRESS (066 XXX)
3: LOAD LAM* (307 - overwrites A)
4: INCREMENT L (060)
5: REPEAT STEPS 3 AND 4

*Address precedes data on front panel by one step

FREQUENTLY USED INSTRUCTIONS

CODE		DESCRIPTION		BYTES
104	**ADL ADH**	JMP	JUMP TO ADDRESS	3
056	**DATA**	LHI	LOAD H IMMEDIATE	2
066	**DATA**	LLI	LOAD L IMMEDIATE	2
050		INH	INCREMENT H	1
060		INL	INCREMENT L	1
051		DCH	DECREMENT H	1
061		DCL	DECREMENT L	1
076	**DATA**	LMI	LOAD MEMORY IMMEDIATE	2
006	**DATA**	LAI	LOAD A IMMEDIATE	2
307		LAM	LOAD A FROM MEM	1
370		LMA	LOAD MEM FROM A	1
300		LAA	NOP (LOAD A WITH A)	1

REGISTERS

0	1	2	3	4	5	6	7
Acc	B	C	D	E	H	L	Memory

STATUS LED MEANINGS

INT	INTERRUPTED (CPU IN STATE T1I)
RUN	RUNNING (CPU IN STATE T1)
STOP	CPU IN STOPPED STATE

LEFT/RIGHT		STATUS
OFF	OFF	READ 1st BYTE OF INSTRUCTION
ON	OFF	MEMORY READ (INSTR. OR DATA)
OFF	ON	I/O OPERATION
ON	ON	MEMORY WRITE

BASE CONVERSIONS

OCTAL	HEX	DECIMAL
1	1	1
2	2	2
4	4	4
10	8	8
20	10	16
40	20	32
100	40	64
200	80	128

SERIAL BOOT LOADER

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          INPUT:
000:113         INP INPORT
001:240         NDA  ; check start bit
002:160 000 000 JTS INPUT

005:026 010     LCI  8
          TIMER:    ; 1 1/2 bit times
007:021         DCC
010:110 007 000 JFZ TIMER

013:036 010     LDI 8 ; grab 8 bits

          DATAIN:   ; get 1 bit
015:113         INP INPORT
016:022         RAL  ;  move to carry
017:301         LAB  ; fetch current byte
020:032         RAR  ; shift in this bit
021:310         LBA  ; save in B

022:026 003     LCI  3 ; delay 1 bit time
          BITTMR:
024:021         DCC
025:110 024 000 JFZ BITTMR

030:300         LAA  ; timing delay
031:031         DCD  ; 8 bits captured?
032:110 015 000 JFZ DATAIN ; no, continue

035:371         LMB  ; store byte
036:060         INL  ; increment pointer
037:110 000 000 JFZ INPUT ; wrap?
042:050         INH  ; increment MSB
043:104 000 000 JMP INPUT ; continue
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1: Toggle in program with front panel
2: Set source to 2400, 8 bits, no parity
3: Set H and L with panel to start addr
4: Set PC to 0
5: Run
6: Send data from source
7: Interrupt when data has been sent
8: Decrement address
9: Using panel, check last byte with LAM

8008 QUICK REFERENCE

REGISTERS

0	1	2	3	4	5	6	7
Acc	B	C	D	E	H	L	Memory

CPU STATES

011	T1I	INTERRUPTED
010	T1	WRITE HIGH ADDRESS
001	T2	WRITE LOW ADDRESS
000	WAIT	MEMORY NOT READY
100	T3	INSTRUCTION OR DATA FETCH
110	STOP	CPU IN STOPPED STATE
111	T4	INSTRUCTION EXECUTION 1
101	T5	INSTRUCTION EXECUTION 2

CYCLE CONTROL DECODES*

00	PCI	READ 1st BYTE OF INSTRUCTION
01	PCR	MEMORY READ (INST. OR DATA)
10	PCC	I/O OPERATION
11	PCW	MEMORY WRITE

*These are the two most significant bits of high address during T1

FLAGS

CARRY	UNSIGNED CARRY OUT/BORROW IN
PARITY	PARITY OF RESULT IS EVEN
SIGN	MOST SIGNIFICANT BIT OF RESULT
ZERO	RESULT EQUALS ZERO

INSTRUCTION SET

CPU CONTROL (FLAGS NOT AFFECTED)

Octal	Opcode	Description	States
000	HLT	halt	4
001	HLT	halt	4
377	HLT	halt	4

INPUT AND OUTPUT (FLAGS NOT AFFECTED)

Octal	Opcode	Description	States
1xx	INP	input port M (0100MMM1)	8
1xx	OUT	output port M (01RRMMM1) RR != 0	6

JUMP AND CALL* (FLAGS NOT AFFECTED)

Octal	Opcode	Description	States
1x4	JMP	unconditional jump	11
100	JFC	jump if carry = 0	9 or 11
110	JFZ	jump if zero = 0	9 or 11
120	JFS	jump if sign = 0	9 or 11
130	JFP	jump if parity = 0	9 or 11
140	JTC	jump if carry = 1	9 or 11
150	JTZ	jump if zero = 1	9 or 11
160	JTS	jump if sign = 1	9 or 11
170	JTP	jump if parity = 1	9 or 11
1x6	CAL	unconditional call subroutine	11
102	CFC	call if carry = 0	9 or 11
112	CFZ	call if zero = 0	9 or 11
122	CFS	call if sign = 0	9 or 11
132	CFP	call if parity = 0	9 or 11
142	CTC	call if carry = 1	9 or 11
152	CTZ	call if zero = 1	9 or 11
162	CTS	call if sign = 1	9 or 11
172	CTP	call if parity = 1	9 or 11

RESTART (FLAGS NOT AFFECTED)

Octal	Opcode	Description	States
0a5	RST	call subroutine at 0a0	5

RETURN (FLAGS NOT AFFECTED)

Octal	Opcode	Description	States
003	RFC	return if carry = 0	3 or 5
013	RFZ	return if zero = 0	3 or 5
023	RFS	return if sign = 0	3 or 5
033	RFP	return if parity = 0	3 or 5
043	RTC	return if carry = 1	3 or 5
053	RTZ	return if result = 1	3 or 5
063	RTS	return if sign = 1	3 or 5
073	RTP	return if parity = 1	3 or 5
0X7	RET	unconditional return	5

*Followed by 2 bytes (low, then high address)

LOAD (FLAGS NOT AFFECTED)

Octal	Opcode	Description	States
3ds	Lds	load d with s	5
3d7	LdM	load d with Memory	8
37s	LMs	load Memory with s	7
0d6	LdI*	load register d with Immediate	8
076	LMI*	load Memory with Immediate	9

ARITHMETIC (ALL FLAGS AFFECTED)

Octal	Opcode	Description	States
20s	ADs	add s to A	5
207	ADM	add Memory to A	8
004	ADI*	add Immediate to A	8
21s	ACs	add s + carry to A	5
217	ACM	add Memory + carry to A	8
014	ACI*	add Immediate + carry to A	8
22s	SUs	subtract s from A	5
227	SUM	subtract Memory from A	8
024	SUI*	subtract Immediate from A	8
23s	SBs	subtract s + carry from A	5
237	SBM	subtract Memory + carry from A	8
034	SBI*	subtract Immed. + carry from A	8
27s	CPs	compare s with A	5
277	CPM	compare Memory with A	8
074	CPI*	compare Immediate with A	8

BOOLEAN (ALL FLAGS AFFECTED, CARRY = 0)

Octal	Opcode	Description	States
24s	NDs	s AND A to A	5
247	NDM	Memory AND A to A	8
044	NDI*	Immediate AND A to A	8
25s	XRs	s XOR A to A	5
257	XRM	Memory XOR A to A	8
054	XRI*	Immediate XOR A to A	8
26s	ORs	s OR A to A	5
267	ORM	Memory OR A to A	8
064	ORI*	Immediate OR A to A	8

INCREMENT/DECREMENT (CARRY NOT AFFECTED)

Octal	Opcode	Description	States
0d0	INd	increment register d (d != A)	5
0d1	DCd	decrement register d (d != A)	5

ROTATE (ONLY CARRY FLAG AFFECTED)

Octal	Opcode	Description	States
002	RLC	rotate A left	5
012	RRC	rotate A right	5
022	RAL	rotate A left through carry	5
032	RAR	rotate A right through carry	5

*Followed by 1 byte (immediate data)